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A 2.4GHz 90nm Single-ended Inductively-Degenerated Interstage Matched Common-source Cascode CMOS LNA

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Abstract—*The LNA is implemented using 90nm CMOS technology. The cascode topology with single-ended source degeneration using inductor is employed. The high gain is achieved by using common-source (CS) amplifier. A different input matching as well as output matching topology may improve the efficiency and minimize noise of the LNA. An inductance network (L_g, L_s) is used for input matching. An interstage inductor between the common source stage and common gate stage is used to increase the overall gain. The amplifier operates at 2.4GHz with an input return loss better than -15 dB. The LNA will have high isolation with voltage gain> 15 dB, NF< 4dB, S21> 20dB and IIP3> −10dBm. The LNA consumes current< 14 mA from a near about 1.2-V supply. The detailed analysis of the proposed LNA will be presented. Experimental measurements explain a correct operation of the circuits, tuning of Noise Fig. (NF), IIP3 and S-parameters. To our knowledge, this is the first architecture that provides all these particulars. This LNA finds its application at Portable GPS Receiver, BLE (Bluetooth Low Energy), Zigbee, NFC, WiFi, Wireless Sensor Network, RFIC operating at 2.4GHz frequency.*

Index Terms*: Inductively-degenerated, Common-source cascode Low Noise Amplifier (LNA), Interstage match, Fig. of Merit (FoM), Input referred third-order intercept point (IIP3), S-parameter.*

1. INTRODUCTION

NOW-A-DAYS, the explorations of CMOS technology have made the vibrant development in the wireless communications circuits, systems area and low cost with least power consumption. Various new communication standards have also been developed to accommodate a variety of applications at different frequency bands, such as cellular communications at 900 and 1800 MHz, Global positioning system (GPS) at 1.2 and 1.5 GHz, and Bluetooth and Wi-Fi at 2.4 and 5.2 GHz, respectively.

The IEEE 802.15.4 i.e. 2.4 GHz is to provide communication over distances about 10m and maximum transfer data rates of 250 kbps. The modern wireless technology is now motivated by the global trend of developing multiband/wideband terminals with multifunction transceivers at low cost.

The first stage of a receiver is LNA whose main function is to provide enough gain to overcome the noise of subsequent stages such as mixer. Aside from providing this gain an LNA should accommodate large signal without distortion and frequently must also present specific impedance of 50Ω to the input source. Since transfer function of many filters are quite sensitive to the quality of termination also being the first stage in the receiver path, its noise Fig. directly adds to that of the system. The purpose of front end LNA is therefore to amplify the received signal to acceptable levels i.e. selectivity while minimizing the noise addition i.e. sensitivity. Due to the process variations the fluctuations in integrated capacitors, resistors and transconductance are about 10% to 20% from their designed values [1]. Also parasitic capacitor and resistor exists in integrated circuits [2, 3]. The introduction of a matching inductor between the two transistors of the cascode structure further improve the gain and noise performance over the commonly used cascode design. An extensive analysis has been carried out to enhance its performance with the inter-stage matching inductor. Single ended topology does not require balun to convert signal from the antenna into a differential signal. A practical balun introduces extra loss which directly adds to the noise Fig. of the system.

In a heterodyne architecture the minimum gain of the LNA is governed by three parameters: the loss of the image–reject filter, the Noise Fig. and IIP3 of the mixer. Stability, matching and reverse isolation are also important parameters of concern. S-parameter shows attenuation of noise and matching in the circuit. Common-source stage exhibits higher drive efficiency than does a source follower. In designing circuits for LNA, the major issue is to minimize noise Fig. as well as to provide a stable 50Ω input match for maximum power transfer.

2. MOTIVATION

The common approach for designing a narrowband LNA is to use a cascode amplifier with inductive degeneration where as the concept of multiband or wideband concurrent receiver [4]

for GPS and Bluetooth application has been used. Fig.1 [5] shows narrowband LNA. This architecture provides simultaneous input matching and low NF. The output tank circuit is tuned to the required band and the input series resonant circuit is adjusted to provide sufficient matching at the desired frequency band.

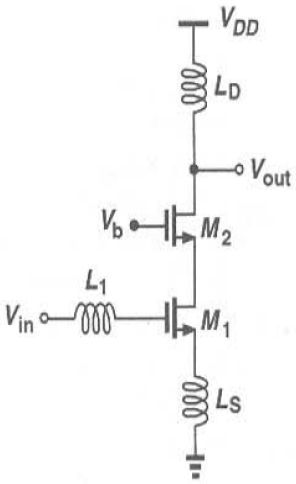

Fig. 1: Basic circuit of CMOS LNA

For this LNA, the input impedance is approximately calculated from [5]

$$Z_{in} = j\omega (L_1+L_s) + (1/j\omega C_{gs}) + \omega_T L_s \quad (1)$$

Where, ω is the frequency of operation in radians per seconds, ω_T is the transistor cut-off frequency in radians per seconds, and C_{gs} is the gate–source capacitance of the main transistor. The real part of the input impedance Z_{in} is adjusted using the source inductor L_s, while the imaginary part is removed at the resonant frequency using the inductor L_1. The NF and the gain at the resonance frequency ω_0 are obtained by [5]

$$NF (\omega_0) = 1+ \chi.\gamma.g_{do} (M1).R_s (\omega_0/\omega_T)^2 \quad (2)$$

$$A (\omega_0) = (R_L/2R_S) (\omega_0/\omega_T) \quad (3)$$

$$\omega_0 = ((1/ (L_1+L_s)C_{gs})^{1/2} \quad (4)$$

Where, g_{do} (M1) is the zero bias drain transconductance of M1, γ is the noise coefficient, χ is the excess noise factor due to the gate noise, R_s is the source resistance and R_L is the load resistance.

The NF defined in (2) is the lowest NF that can be obtained from this architecture, while the input is perfectly matched and the output is tuned to the operating frequency [5]. The same conclusion holds for the gain defined in (3). These results indicate that the performance of the narrowband LNA depends on the resonant frequency, which is adjusted using the inductor L_1 at the input matching network and inductor L_D & capacitor at the output tank circuit.

LNA CONCEPT, TOPOLOGY AND NOISE FIGURE

Conceptually LNA can be foreseen as a cascade of three blocks as the input matching network, amplifier and an output matching network as shown in the Fig.2.

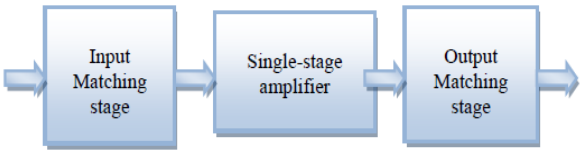

Fig. 2: Concept of LNA

LNA is fabricated using the different MOS topologies that act as an amplifier along with the biasing circuitry. LNA design practice using resistors is generally avoided to have low noise Fig. [2]. Noise Fig. of the first stage greatly decreases the Noise Fig. of system, as this is validated by Frii's equation:

$$F = F_1+ (F_2-1)/A_{12} + (F_3-1)/A_{12}.A_{22} \quad (5)$$

Thus, it becomes very important to have as low Noise Fig. as possible for the first stage.

3. PROPOSED LNA ARCHITECTURE

The proposed architecture is of single-ended cascade type having good frequency response offered by common-gate (CG), also high input resistance and transconductance provided by common-source (CS) amplifier [2, 5] as shown in Fig.3.

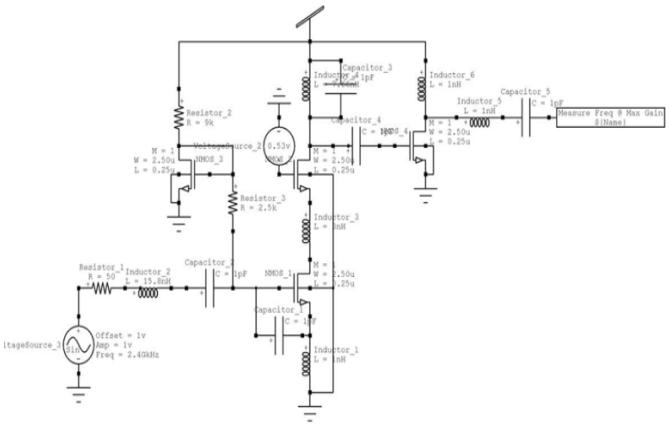

Fig. 3: Inductively degenerated Interstage matched CS cascade LNA.

A. LNA DESIGN & INPUT MATCHING THEORY

Cascode architecture has been used to increase forward gain while decreasing the reverse gain and providing better isolation between input and output ports [5]. Inductive source degeneration is used for input impedance matching and improves stability. This also increases the stability of the LNA through negative feedback at the expense of lower gain.

At resonance, the input resistance is [2]

$$R_{in} = R_e [Z_{in}] = G_m L_s / C_{gs} \quad (6)$$

Indicating that the combination of the transistor with the degeneration inductor provides input matching.

Also at this frequency,

$$\omega^2 (L_g + L_s) C_{gs} = 1 \quad (7)$$

The gain of the LNA in Fig. is given by the following,

$$(V_{OUT}/V_{IN}) = (-G_m.s.L_d) / (1-\omega^2 Cgs(L_g+L_s)+s.L_s.G_{m)} \quad (8)$$

And when substituting (7) into (8) will give

$$(V_{OUT}/V_{IN}) = (-L_d/L_s) \quad (9)$$

$$\text{Thus, Gain} = 20 \log (V_{OUT}/V_{IN}) \text{ dB} \quad (10)$$

This expression shows that the gain is the ratio of the inductor at the drain to the inductor at the source. A high gain can be achieved if L_d is made much higher than L_s. However, there exist a trade-off between the size of L_d and the output performance of the circuit due to the series resistance of the inductor.

The initial stage was to determine the size of the transistor. This was achieved by adopting the power constrained noise optimization method which uses the following equation in determining the width of M1 [1].

$$W_{opt} \approx 1.5(\omega_o L C_{ox} R_s Q_{in\ opt,PD})^{-1} \quad (11)$$

Where, W_{opt} is the optimum width of the transistor having the lowest noise Fig. (NF), L is the length of the transistor, C_{ox} is the oxide capacitance, R_s is the source (input) resistance and $Q_{in\ opt,PD}$ is the input circuit quality factor which equals to 4 as obtained from the derivation [2]. W_{opt} was then calculated. Once width is known, M1's transconductance and C_{gs} can be calculated from the general equations for MOSFETs in saturation.

Capacitance C1 is linked to terminals of M1 in order to reduce value of input matching inductor L_g. Input match condition for the desired band is obtained by utilizing inductors L_s and L_g along with capacitor C2.

B. PRINCIPLE OF INTERSTAGE IMPEDANCE MATCHING & REVERSE ISOLATION

The introduction of an interstage inductor enhances the gain of the cascode LNA. Thus Lin serves as inter-stage matching between drain of M1 and source of M2 i.e. improve intermediate node power transfer. Also, the reduction of Z_{in} due to inclusion of Lin allows more current to pump toward the M2. Therefore, the inter-stage inductor LNA can provide more gain and less miller effect. It will also help to improve the output matching. An inter-stage inductor is thus added between the common- source and common-gate stage. Because of good power transfer in the common-gate stage, the overall noise Fig. will be decreased [9].

It must be noted that with change in Lin, the interstage inductor, the input impedance of M1 changes, hence the input matching network must be readjusted to yield 50Ω impedance. The gain improvement with Lin can explain intuitively. With increase in Lin increase the value of 'C'; that effectively reduces the value of 'F' and voltage gain of amplifier improves with Lin.

Above analysis shows that, the interstage LNA can be further enhanced by increasing the inductor value (Lin). However, use of high value inductor is constrained by the requirement of larger silicon area, limited quality factor and low resonance frequency. The fully on-chip realization of the circuit limits the maximum achievable value of Lin. We thus choose Lin depending on the gain requirement.

The presence of Lin enhances the effective transconductance and effective Quality factor of the circuit. As a result, noise performance improves. This improvement is more pronounced if the inter-stage matching inductor is off chip, thus avoiding large parasitic capacitance. However for on chip realization of the inductor the noise associated with the series resistance tends to cancel the noise improvements and thus keeps the noise performance unchanged. Also enhancing the C_{gd} feed-through causes degradation of reverse isolation, implies decrease in LNA stability due to mutual coupling. So inter-stage inductor increases the gain but at the cost of lower stability factor.

M3and R1form a current mirror circuit with M1. R3 isolates the signal path from the biasing circuit and in this way enforces the input signal to the LNA input. The value of R3 is not critical as long as it is much greater than the input impedance of the stage prior to it. In this work R3 is 2.5 kΩ [2].

Typically, single transistor M1 is sufficient to provide amplification. Adding M2 improves isolation and increases the gain and as a consequence Noise Fig. and linearity get deteriorated. Stability of the circuit is determined by the Stern's stability factor which is given as:

$$K = (1+|\Delta|^2-|S_{11}|^2-|S_{22}|^2) / (2|S_{21}||S_{12}|) \quad (12)$$

Where, $\Delta = S_{11}.S_{12}-S_{21}.S_{22}$

C. OUTPUT MATCHING THEORY

M4 lowers the local oscillator leakage produced by the following mixer and improves the stability of the circuit by minimizing the feedback from the output to the input [6]. An analog output buffer is incorporated with the LNA to get a better output matching response across all the frequency bands. L_d and C_d provides output matching. Besides this, their combination at resonance enables additional filtering to the output. In addition to these, the voltage drop across the

inductor is contributed by its series resistance only and hence, this configuration is very attractive for low power design.

4. LINEARIZATION OF THE PROPOSED LNA

Out of the available techniques for linearization of LNAs' [10], techniques that target improvising IIP3 only are Feedback, Optimal Biasing, Harmonic Termination, Feed-forward, Derivative Superposition, etc. Every technique targets the nonlinear G_m3 characteristics of MOS, and try to fetch linearization at point when MOS swings from sub-threshold to saturation region. Gm of MOS in saturation is given as:

$$G_m = (\partial I_d / \partial V_{GS}) \mid V_{DS}, \text{constant} \quad (13)$$

$$G_m = \mu_n Cox\ (W/L)\ (V_{GS}\text{-}Vt) \quad (14)$$

The linearity of the amplifier is measured by the input-referred third-order intercept point (IIP3). The IIP3 is inversely proportional to square of the effective Quality factor of input tuning circuit. Hence the inclusion of Lin causes the linearity performance of the LNA to deteriorate. IIP3 in terms of Gm1and Gm3is given as:

$$IIP3 = ((4 \mid G_m1 \mid)/ (3 \mid G_m3 \mid))^{1/2} \quad (15)$$

5. SIMULATION AND EXPERIMENTAL RESULTS

The proposed CMOS LNA has been simulated in 90nm using TANNER simulator. The Noise Fig. of LNA can be reduced by the following factors: (1) improving the quality factor (Q) of the on-chip inductors as parasitic parameters like eddy current loss, parasitic capacitance induced by skin effect of inductor and thermal noise of parasitic impedance of the circuit. (2) Channel noise factor γ of short-channel MOS device is related to the biasing network; (3) the thermal noise of gate resistance of MOSFET also contributes to the output noise of the LNA. Much better performance of the proposed architecture can be expected if the design is implemented in advanced RF substrates.

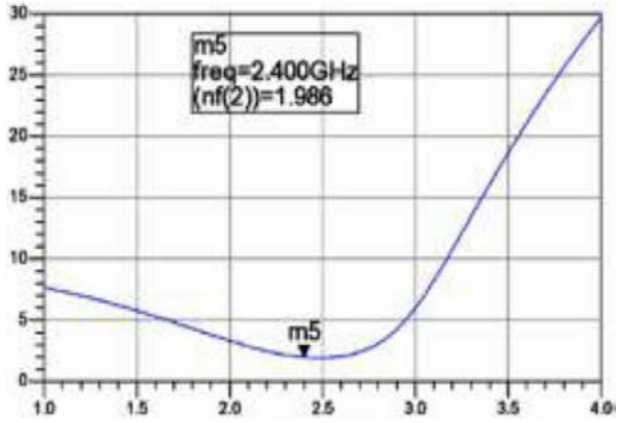

Fig. 4: Noise Fig. of the LNA (Minimum Noise Fig. is 1.986 dB at 2.4 GHz).

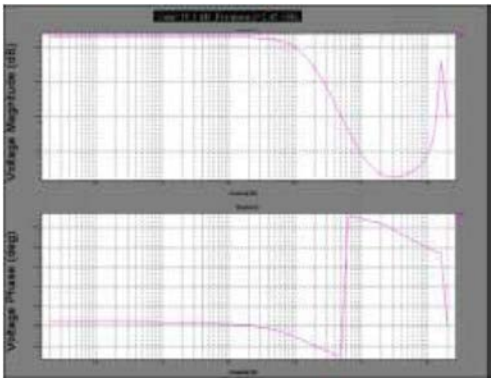

Fig.5: Voltage magnitude (19.1dB) and Phase magnitude (deg) at 2.4 GHz.

6. 6. CONCLUSION

This paper also shows the effect of inter-stage matching and shows that the addition of the inter-stage matching inductor increases gain. The cascode topology at the first stage with source degeneration inductor and common-source (CS) amplifier help to increase the gain. The proposed LNA is suitable for high gain and high linearity Bluetooth receivers. The design and implementation of 1.2V 90nm CMOS LNAs has been presented. Experimental measurements have been included, showing a competitive behaviour as compared with the state-of-the art on narrowband LNAs. From the charts we can seen that the LNA has sufficient gain along with the noteworthy values of Noise Figure. IIP3 achieves optimize value which is sufficiently enough to suppress unwanted third order inter-modulations at the output of the LNA circuit. Fig. of Merit i.e. FoM for LNA circuits is given as:

$$FoM = (\mid S_{21} \mid .BW) / ((NF\text{-}1).P_{DC}) \quad (16)$$

A comparison table show the comparison of different LNA works formerly accomplished along with the work presented in this paper. From the table we can easily observe that the work carried out in this paper gives least value of noise Fig. and also has comparatively superlative value of IIP3.

Table I: PERFORMANCE SUMMARY OF THE PROPOSED LNA AND COMPARISON WITH THE EXISTING WORK

REFERENCES	Freq. Range (GHz)	Gain(dB)	NF(dB)	IIP3(dBm)	Pdc(mW)	VDD(V)	Technology (CMOS)
[4]	2.4583	14	2.3	0	10	2.5	350nm
[5]	1.5	-	3.5	12.7o/p	7.5	1.5	600nm
[6]	2.4	23.9	5.6	-11.1	8.1	1.2	130nm
[9]	2.4-2.48	19	2.4	-	9	3	500nm
[11]	2.4	22.1	1.47	-8.1	11.1	1.8	180nm
[12]	2.44	-	1.77	-0.6	25.3	1	90nm
This Work	2.4	19.1	1.986	>-10	<16	1.2	90nm

Table II: LNA Specifications

Standard BW(GHz) NF(dB) S_{21}(dB) IIP3 (dBm)
GSM 1.85-1.99 1.7 11.5 -2
WCDMA 1.92-2.17 3.7 18 -0.5
Bluetooth 2.4-2.4835 2.8 12.5 -12
WLAN 2.4-2.4835 4.5 19.6 -5.4

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